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Patentanmeldung Nr. Patent application No. Demande de brevet n°

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Der Präsident des Europäischen Patentamts;
Im Auftrag

For the President of the European Patent Office

Le Président de l'Office européen des brevets
p.o.

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(Falls die Bezeichnung der Erfindung nicht angegeben ist, siehe Beschreibung.
If no title is shown please refer to the description.
Si aucun titre n'est indiqué se referer à la description.)

Data communication

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Data communication

The invention relates to a system including a signal or data bus, and in particular to a method and apparatus for reducing ground bounce in the buses of high speed, high density integrated circuits that use fault tolerant error correcting codes.

As integrated circuit technology is scaled to provide increased density on a chip, the on-chip interconnects tend to become narrower and narrower. These trends lead to an increase in coupling capacitance with neighboring wires, which in turn leads to increased interference or crosstalk between wires.

One problem for integrated circuit technology, and particularly for deep submicron and high-speed designs, is 'ground bounce'. Drivers of an output buffer connected to an off-chip interconnect have to deliver large currents to charge the highly capacitive loads. When drivers switch simultaneously, the large current drawn causes a drop in the supply voltage. Likewise, when the buffers have to discharge the external lines, a large amount of charge is dumped on the ground plane. This may cause the voltage of the ground plane to rise. The reduced voltage difference between the supply and ground plane causes a reduced noise margin and a reduced speed. Hence an integrity problem arises.

It is known in the art that 'ground bounce' can be reduced by increasing the AC and DC stability of the circuit. AC stability is achieved when the number of transitions from a first state to a second state equals the number of transitions from the second state to the first state. DC stability is achieved when the number of first states equals the number of second states.

The document "Balanced LVD SCSI Drivers and Receivers" by The SCSI Trade Association from Computer Technology Review, September 1997 shows a Balanced LVD Driver that has a reduced ground bounce and a reduced simultaneous switching current.

If the environment in which a bus or communication channel transfers data to a circuit is prone to errors, it is desirable to provide means for correcting errors in the code used to transmit the data. Such a bus or communication channel is said to be fault tolerant.

Figure 1 shows a schematic illustration of a typical fault tolerant bus structure 1. The bus structure 1 comprises a communication bus 3 for communicating data between an encoder 5 and decoder 7. The bus 3 receives output data 9 from the encoder 5, and provides input data 11 to the decoder 7.

One fault tolerant method is known as 'dual-rail encoding'. In dual-rail encoding, a data bit is copied, and the copy can be used to correct errors in the data bit. Incidentally, as the data bit and copy bit are the same, the crosstalk between the two wires carrying the data and copy bits will be eliminated.

Figure 2 shows a prior art dual-rail bus structure 20. The input data bits d0, d1, d2 and d3 are the signals provided to the encoder 22. Respective copies c0, c1, c2 and c3 of the data bits d0, d1, d2 and d3 are created. A parity bit, Tparity, is calculated for the data bits to be transmitted using a parity tree 24 comprising, for example, exclusive OR gates 26, 28 and 30.

The transmitted data parity bit, Tparity, data bits d0, d1, d2 and d3, and their copies c0, c1, c2 and c3 are transmitted over a communications bus 32 to a decoder 34.

During transmission, the transmitted data bits and their copies may become 'faulty', that is, the transmitted bit may be detected as a '1' instead of a '0', or vice versa. Therefore, the data bits D0, D1, D2 and D3 and the copies C0, C1, C2 and C3 received at the decoder 34 may, or may not, be the same as the data bits d0, d1, d2 and d3 and copy bits c0, c1, c2, c3 transmitted by the encoder 22. A received data parity bit, Rparity, is calculated for the data bits D0, D1, D2 and D3 received from the communications bus 32 by parity tree 36, which is identical in structure to parity tree 24 in the encoder 22. A multiplexer control bit, s0, is determined by comparing the received data parity bit, Rparity, with the transmitted data parity bit, Tparity, received over the communications bus 32. In this illustrated system, the comparison is performed by an exclusive OR gate 38.

The multiplexer control bit s0 is fed into a plurality of multiplexers Mux0, Mux1, Mux2 and Mux3 that act as correction circuits. Each multiplexer Mux0, Mux1, Mux2 and Mux3 receives a respective received data signal D0, D1, D2 or D3 and a corresponding received copy of the data signal C0, C1, C2 or C3. The multiplexer control bit s0 controls whether each multiplexer outputs the received data signal or the received copy of the data signal.

When the received data parity bit, Rparity, is the same as the transmitted data parity bit, Tparity, the multiplexer control bit s0, is a '0', which instructs the multiplexers

the received data parity bit, Rparity, is different to the transmitted data parity bit, Tparity, the multiplexer control bit, s0, is a '1', which instructs the multiplexers Mux0, Mux1, Mux2 and Mux3, to output the received copies of the transmitted data bits C0, C1, C2 and C3.

However, as there are twice as many wires switching at any one time in a dual-rail encoding system compared with a single-rail system, the problem of ground bounce is increased.

There is therefore a need to reduce or eliminate ground bounce in integrated circuits that use a fault tolerant code for transmitting data across a data bus, and in particular in systems that use dual-rail encoding.

Therefore, according to a first aspect of the present invention, there is provided a module for transmitting a plurality of data bits to another module via a communication bus, the module comprising: means adapted to generate respective copies of the data bits; means adapted to invert the respective copies of the data bits; and means adapted to transmit, via the communication bus, the plurality of data bits and their respective inverted copies to the other module.

Preferably, the module has means for generating a first parity bit from the plurality of data bits, wherein the means adapted to transmit is further adapted to transmit, with the plurality of data bits and their respective inverted copies, the first parity bit to the other module.

Preferably, the means for generating a first parity bit comprises one or more logic gates.

Preferably, the module further comprises means adapted to generate an inverted copy of the first parity bit and wherein the means adapted to transmit is further adapted to transmit, with the plurality of data bits, their respective inverted copies and the first parity bit, the inverted copy of the first parity bit to the other module.

According to a second aspect of the present invention, there is provided a module for receiving a plurality of data bits from another module via a communication bus, the module comprising: means adapted to receive the plurality of data bits and respective inverted copies of the data bits from the other module; means adapted to detect the presence of one or more errors in the received data bits; means adapted to select the received data bits as the output of the module in the event that the means adapted to detect the presence of one or more errors does not detect any errors, and to select the inverse of the respective received

inverted copies of the data bits as the output of the module in the event that the means adapted to detect detects the presence of one or more errors.

Preferably, the means adapted to receive is further adapted to receive a first parity bit from the other module, and the module further comprises means for generating a second parity bit from the received data bits, and wherein the means adapted to detect the presence of one or more errors in the received data bits is adapted to compare the first and second parity bits.

Preferably, the means for generating a second parity bit comprises one or more logic gates.

Preferably, the means adapted to detect the presence of one or more errors in the received data bits comprises a logic gate.

Preferably, the means adapted to select comprises one or more multiplexers, each multiplexer having a received data bit and the inverse of its respective received inverted copy as inputs, with each multiplexer being operable in response to a control signal output by the means adapted to detect.

Alternatively, the means adapted to select comprises one or more multiplexers, each multiplexer having the inverse of a received data bit and its respective received inverted copy as inputs, with each multiplexer being operable in response to a control signal output by the means adapted to detect, and wherein the output of the module is the inverse of the output of each multiplexer.

According to a third aspect of the present invention, there is provided a system comprising a module adapted to transmit as described above, and a module adapted to receive as described above, the modules being connected via a communication bus.

According to a fourth aspect of the present invention, there is provided a method of reducing ground bounce in a system in which a plurality of data bits are to be transmitted from a first module to a second module via a communication bus; the system being able to detect errors in the received data bits; the method comprising: in the first module: generating respective copies of the data bits to be transmitted; inverting the respective copies of the data bits; and transmitting, via the communication bus, the plurality of data bits and their respective inverted copies to the second module.

Therefore, as each line in the communication bus carrying a data bit has a corresponding line carrying an inverted copy of the data bit, the number of lines carrying a high signal will be the same as the number of wires carrying a low signal (ensuring DC [illegible]

low signal will be the same as the number of transitions from a low signal to a high signal (ensuring AC stability).

Preferably, in the second module, the plurality of data bits and their respective inverted copies are received from the first module, the presence of one or more errors in the received data bits is determined, the received data bits are used as the output of the second module in the event that one or more errors are not detected in the received data bits, and the respective copies of the data bits are used as the output of the second module in the event that one or more errors are detected in the received data bits.

Preferably, in the first module, a first parity bit is generated from the plurality of data bits to be transmitted and the first parity bit is transmitted to the second module with the plurality of data bits and their respective inverted copies.

Preferably, in the second module, the first parity bit is received from the first module a second parity bit is generated from the received data bits and the step of detecting one or more errors in the received data bits comprises comparing the first and second parity bits.

Preferably, in the first module, an inverted copy of the first parity bit is generated and transmitted to the second module with the plurality of data bits, their respective inverted copies and the first parity bit.

For a better understanding of the present invention, and to show more clearly how it may be carried into effect, reference will now be made, by way of example, to the following drawings, in which:

Figure 1 is a schematic illustration of a typical fault tolerant bus structure.

Figure 2 shows a prior art dual-rail bus structure.

Figure 3 shows a system using dual-rail encoding according to a first embodiment of the present invention.

Figure 4 shows an alternative system using dual-rail encoding according to the first embodiment of the present invention.

Figure 5 shows a system using dual-rail encoding according to a second embodiment of the present invention.

Figure 6 is a flow chart illustrating a method of reducing ground bounce according to the invention.

In the prior art dual-rail encoder described above, copies of the input data bits d0, d1, d2 and d3 are generated in a first module, and these copies are used to correct errors that are detected in received data bits by a second module.

As each data line in the output of the first module to a communication bus has a corresponding line carrying an identical copy of the signal on the data line, the problem of ground bounce is increased relative to systems that do not use copies of the data bits.

For example, consider a four-line bus with each data line having a high signal (i.e. 1 1 1 1). If there is a transition on each of the data lines to a low signal (i.e. 0 0 0 0) then a significant amount of charge will be dumped onto the ground plane, causing 'ground bounce'.

Now, if the four-line bus uses dual-rail encoding, there will be additional lines for each of the four data lines, each carrying a copy of the signal on their respective data line. Therefore, if each data line carries a high signal (and hence each copy line also carries a high signal) then a transition of each data line from a high signal to a low signal will result in eight lines discharging to the ground plane, causing twice as much 'ground bounce' as in a normal four-line bus.

Therefore, in accordance with the invention, the problem of ground bounce in a structure that uses dual-rail encoding is reduced by increasing the AC and DC stability of the code used to transmit the data. That is, AC and DC stability is achieved when the number of lines transitioning from a high signal to a low signal is the same as the number of lines transitioning from a low signal to a high signal; and the number of lines carrying a high signal is the same as the number of lines carrying a low signal.

Figure 3 shows a system using dual-rail encoding according to a first embodiment of the present invention. In the system 50, there are four input data rails carrying data bits d0, d1, d2 and d3.

As described above, in addition to the data lines carrying data bits d0, d1, d2 and d3, there are provided lines that carry respective copies c0, c1, c2 and c3 of the data bits.

However, in accordance with the invention, the AC and DC stability of the system 50 is increased by inverting the signals on the lines that carry the respective copies of the data bits before transmission of the data across communication bus 54.

Therefore, respective copies c0, c1, c2 and c3 of the data bits are inverted by respective inverters [illegible] and these respective inverted copies are denoted [illegible]

As each line to the communication bus 54 carrying a data bit has a corresponding line carrying an inverted copy of the data bit, the number of lines carrying a high signal will be the same as the number of wires carrying a low signal. Therefore, the output of the first module 52 is DC stable. When transitions occur, as any data bit transitioning from a first state to the second state will be accompanied by its respective inverted copy transitioning from the second state to the first state, the number of transitions from a high signal to a low signal will be the same as the number of transitions from a low signal to a high signal. Therefore, the output of the first module 52 is AC stable. Hence, the problem of ground bounce in the communication bus 54 caused by transitions on the data lines has been reduced.

The data bits d0, d1, d2 and d3 and their respective inverted copies c0', c1', c2' and c3', forming the output of the first module 52, are transmitted to a second module 56 via the communication bus 54.

It should be noted that the first and second modules 52, 56 may not be separate circuit components from the communication bus 54, but they may form a single integrated unit. Specifically, the first module 52 may be the driver for the communication bus 54, and the second module 56 may be the receiver.

During transmission across the communication bus 54, the transmitted data bits and their respective inverted copies may become 'faulty', that is, the transmitted bit may be detected as a '1' instead of a '0', or vice versa. Therefore, data bits D0, D1, D2 and D3 and the respective inverted copies C0', C1', C2' and C3' received at the second module 56 may, or may not, be the same as the data bits d0, d1, d2 and d3 and respective inverted copy bits c0', c1', c2', c3' transmitted by the first module 52.

In a preferred embodiment, in order for the second module 56 to detect errors in the received data bits D0, D1, D2 and D3, a parity bit, Tparity, is calculated by the first module 52 and provided to the second module 56. This parity bit is calculated in the first module 52 for the data bits to be transmitted using parity tree 58, which, in this illustrated embodiment, comprises exclusive OR gates 60, 62 and 64. However, it will be appreciated that the parity tree 58 may comprise other combinations of logic gates.

The first module 52 then transmits the transmitted data parity bit, Tparity, to the second module 56 along with data bits d0, d1, d2 and d3, and their respective inverted copies c0', c1', c2' and c3' via the communications bus 54.

The second module 56 calculates a received data parity bit, Rparity, for the received data bits D0, D1, D2 and D3. The received parity bit, Rparity, is calculated using parity tree 66, which is identical in structure to parity tree 58 in the first module 52.

The second module 56 then compares the received data parity bit, Rparity, with the transmitted data parity bit, Tparity, received over the communications bus 54. In this illustrated embodiment, the comparison is performed by exclusive OR gate 68, although it will be appreciated that the comparison may be performed by other types of logic gates. The output of the exclusive OR gate 68 is a multiplexer control bit s0.

The multiplexer control signal s0 is fed into a plurality of dual-input multiplexers Mux0, Mux1, Mux2 and Mux3 that act as correction circuits for the second module 56. Each multiplexer, Mux0, Mux1, Mux2 and Mux3 receives a respective received data bit D0, D1, D2 or D3 and a corresponding received inverted copy of the data bit C0,' C1', C2' or C3'.

As is conventional, the multiplexer control bit s0 determines which of the signals input into the multiplexer is to be used as the output of the multiplexer. When the multiplexer control bit is low (i.e. a '0'), the output of the multiplexer will be the received data bit. However, when the multiplexer control bit is high (i.e. a '1'), the output of the multiplexer will be the received inverted copy of the associated data bit.

However, it will be appreciated that, in order for errors in the received data bits D0, D1, D2 and D3 to be corrected by the multiplexers Mux0, Mux1, Mux2 and Mux3, the received inverted copies of the data bits C0', C1', C2' and C3' must be inverted relative to the received data bits.

A first structure for achieving this is shown in Figure 3. Here, each received data bit D0, D1, D2 and D3 is inverted by respective inverters 700, 701, 702 and 703 before they are input into the respective multiplexers Mux0, Mux1, Mux2 and Mux3. Since the output of the multiplexers is now the inverse of the desired signal, further inverters 720, 721, 722 and 723 invert the outputs of the multiplexers Mux0, Mux1, Mux2 and Mux3 respectively to form the output signals of the second module 56, namely, signals out0, out1, out2 and out3.

Figure 4 shows an alternative structure for inverting the received inverted copies of the data bits relative to the received data bits. Here, each received inverted copy C0', C1', C2' and C3' is inverted by respective inverters 740, 741, 742 and 743 before they are input into the respective multiplexers Mux0, Mux1, Mux2 and Mux3.

Therefore, in both of these structures, when the received data parity bit, Rparity, is the same as the transmitted data parity bit, Tparity, the multiplexer control bit s0 is a '0', which instructs the multiplexers Mux0, Mux1, Mux2 and Mux3, to output the received data bits D0, D1, D2 and D3. However, when the received data parity bit, Rparity, is different to the transmitted data parity bit, Tparity, (and hence that the received data bits D0, D1, D2 and/or D3 are different to the transmitted data bits d0, d1, d2, and d3) the multiplexer control signal s0 is a '1', which instructs the multiplexers Mux0, Mux1, Mux2 and Mux3, to output the received copies of the transmitted data bits C0, C1, C2 and C3.

It will be appreciated that in the dual-rail encoding system described above, where a parity bit is transmitted to the second module along with the data bits and their respective inverted copies, the transmission is not perfectly AC and DC stable.

Therefore, in accordance with a second embodiment of the present invention, the first module generates an inverted copy of the transmitted data parity bit, Tparity, and transmits this to the second module, along with the data bits, their respective inverted copies, and the transmitted data parity bit.

A system in accordance with the second embodiment of the present invention is shown in Figure 5. In Figure 5, features that are common to the first embodiment of the invention (illustrated in Figures 3 and 4) are given the same reference numeral.

As described above, to achieve perfect AC and DC stability in the transmission across the communication bus 54, the transmitted data parity bit, Tparity, is copied, inverted (by inverter 76) and is transmitted across the communication bus 54 to the second module 56. Therefore, since every data line has an inverse copy, and the transmitted parity bit has an inverse copy, the transmission is perfectly AC and DC stable. Therefore, the problem of ground bounce caused by transitions at the communication bus 54 is reduced.

In the second module 56, the inverse copy of the transmitted parity bit, Tparity', is discharged to the ground plane via a resistor 78.

Figure 6 is a flow chart illustrating the method of reducing ground bounce according to the invention. In step 1002, copies of data bits that are to be transmitted from a first module to a second module across a communication bus are generated.

In step 1004, the copies of the data bits are inverted. i.e. for a data bit having a value '0', the inverted copy will have a value '1'.

In step 1006, the copies of the data bits and the original data bits are transmitted via the communication bus to the second module.

Therefore, the problem of ground bounce in a structure that uses dual-rail encoding is reduced as the AC and DC stability of the code used to transmit the data is increased.

The second module receives, via the communication bus, the plurality of data bits and their respective inverted copies from the first module and detects the presence of one or more errors in the received data bits. If no errors are detected in the received data bits, the received data bits are used as the output of the second module. However, if one or more errors are detected in the received data bits, the respective copies of the data bits are used as the output of the second module.

Preferably, a first parity bit may be generated from the plurality of data bits to be transmitted, and the first parity bit is transmitted to the second module with the plurality of data bits and their respective inverted copies.

At the second module, the first parity bit is received. The second module then generates a second parity bit from the received data bits. This second parity bit can then be compared with the received first parity bit to determine whether there are one or more errors in the received data bits.

To further reduce the ground bounce of the system according to the present invention, an inverted copy of the first parity bit can be generated in the first module. This inverted copy of the first parity bit can be transmitted to the second module with the plurality of data bits, their respective inverted copies and the first parity bit.

Although the invention has been described and illustrated with reference to a system that uses dual-rail encoding, it will be appreciated that the invention is not limited to such systems, and that many other applications of the invention will be apparent to a person skilled in the art.

Furthermore, although the invention has been described and illustrated with reference to a system having four data lines, it will be appreciated that the invention is applicable to systems which have more or less than four data lines.

There is therefore provided a method and system in which the ground bounce in a communication bus is reduced.

It should be noted that the above-mentioned embodiments illustrate rather than limit the invention, and that those skilled in the art will be able to design many alternative embodiments without departing from the scope of the appended claims. The word 'comprising' does not exclude the presence of elements or steps other than those listed in a

CLAIMS:

1. A module for transmitting (52) a plurality of data bits (d0,d1,d2,d3) to another module (56) via a communication bus (54), the module (52) comprising:

- means adapted to generate respective copies (c0,c1,c2,c3) of the data bits;
- means (520,521,522,523) adapted to invert the respective copies of the data bits; and
- means adapted to transmit, via the communication bus (54), the plurality of data bits and their respective inverted copies (c0',c1',c2',c3') to the other module (56).

2. A module (52) as claimed in claim 1, further comprising:

- means (58) adapted to generate a first parity bit (Tparity) from the plurality of data bits (d0,d1,d2,d3);

wherein the means adapted to transmit is further adapted to transmit, with the plurality of data bits (d0,d1,d2,d3) and their respective inverted copies (c0',c1',c2',c3'), the first parity bit (Tparity) to the other module (56).

3. A module (52) as claimed in claim 2, wherein the means (58) adapted to generate a first parity bit comprises one or more logic gates (60,62,64).

4. A module (52) as claimed in claim 2 or 3, further comprising:

- means (520,521,522,523) adapted to generate an inverted copy of the first parity bit (Tparity);

wherein the means adapted to transmit is further adapted to transmit, with the plurality of data bits (d0,d1,d2,d3), their respective inverted copies (c0',c1',c2',c3') and the first parity bit (Tparity), the inverted copy of the first parity bit (Tparity') to the other module (56).

5. A module (56) for receiving a plurality of data bits (D0,D1,D2,D3) from another module (52) via a communication bus (54), the module (56) comprising:

- means adapted to receive the plurality of data bits (D0,D1,D2,D3) and respective inverted copies (C0',C1',C2',C3') of the data bits from the other module (52);

- means (68) adapted to detect the presence of one or more errors in the received data bits (D0,D1,D2,D3);
- means (Mux0,Mux1,Mux2,Mux3) adapted to select the received data bits (D0,D1,D2,D3) as the output of the module (56) in the event that the means (68) adapted to detect the presence of one or more errors does not detect any errors, and to select the inverse of the respective inverted copies (C0',C1',C2',C3') of the data bits as the output of the module (56) in the event that the means (68) adapted to detect detects the presence of one or more errors.

6. A module (56) as claimed in claim 5, wherein the means adapted to receive is further adapted to receive a first parity bit (Tparity) from the other module (52); and wherein the module (56) further comprises:

- means (66) adapted to generate a second parity bit (Rparity) from the received data bits; and

wherein the means (68) adapted to detect the presence of one or more errors in the received data bits is adapted to compare the first and second parity bits.

7. A module (56) as claimed in claim 6, wherein the means (68) adapted to generate a second parity bit (Rparity) comprises one or more logic gates.

8. A module as claimed in 6 or 7, wherein the means (68) adapted to detect the presence of one or more errors in the received data bits comprises a logic gate.

9. A module (56) as claimed in claim 5, 6, 7 or 8, wherein the means (Mux0,Mux1,Mux2,Mux3) adapted to select comprises one or more multiplexers, each multiplexer having a received data bit and the inverse of its respective inverted copy as inputs, and wherein each multiplexer is operable in response to a control signal (s0) output by the means (68) adapted to detect.

10. A module (56) as claimed in claim 5, 6, 7 or 8, wherein the means (Mux0,Mux1,Mux2,Mux3) adapted to select comprises one or more multiplexers, each multiplexer having the inverse of a received data bit and its respective inverted copy as inputs, and wherein each multiplexer is operable in response to a control signal (s0) output by

the means (68) adapted to detect, and wherein the output of the module (56) is the inverse of the output of each multiplexer.

11. A system comprising a module for transmitting (52) as claimed in one of claims 1 to 4 and a module for receiving (56) as claimed in one of claims 5 to 10, the modules being connected via a communication bus (54).

12. A method of reducing ground bounce in a system in which a plurality of data bits are to be transmitted from a first module to a second module via a communication bus, the system being able to detect errors in the transmitted data bits, the method comprising:

- generating respective copies of the data bits to be transmitted (step 1002);
- inverting the respective copies of the data bits (step 1004); and
- transmitting, via the communication bus, the plurality of data bits and their respective inverted copies to the second module (step 1006).

13. A method as claimed in claim 12, the method further comprising:

- receiving, via the communication bus, the plurality of data bits and their respective inverted copies from the first module;
- detecting the presence of one or more errors in the received data bits;
- using the received data bits as the output of the second module in the event that one or more errors are not detected in the received data bits;
- using the respective copies of the data bits as the output of the second module in the event that one or more errors are detected in the received data bits.

14. A method as claimed in claim 12 or 13, the method further comprising:

- generating a first parity bit from the plurality of data bits to be transmitted; and
- transmitting the first parity bit to the second module with the plurality of data bits and their respective inverted copies.

15. A method as claimed in claim 14, the method further comprising:

- receiving, via the communication bus, the first parity bit from the first module;
- generating a second parity bit from the received data bits;
- wherein the step of detecting one or more errors in the received data bits comprises comparing the first and second parity bits.

16. A method as claimed in claim 14 or 15, the method further comprising:

- generating an inverted copy of the first parity bit; and
- transmitting the inverted copy of the first parity bit to the second module with the plurality of data bits, their respective inverted copies and the first parity bit.

ABSTRACT:

There is provided a first module for transmitting a plurality of data bits to a second module via a communication bus with reduced ground bounce, the first module comprising means adapted to generate respective copies of the data bits; means adapted to invert the respective copies of the data bits; and means adapted to transmit, via the communication bus, the plurality of data bits and their respective inverted copies to the second module. A parity signal and an inverted copy thereof may also be transmitted between the first module and the second module.

Fig. 3

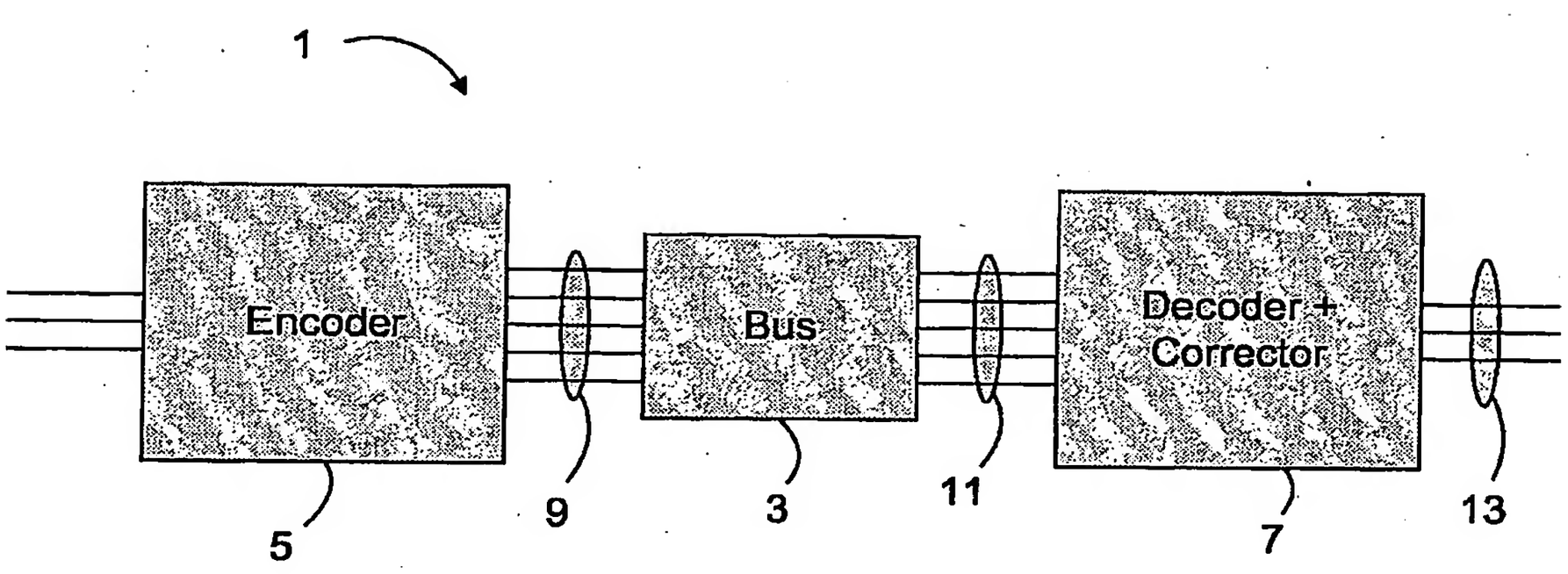

FIGURE 1

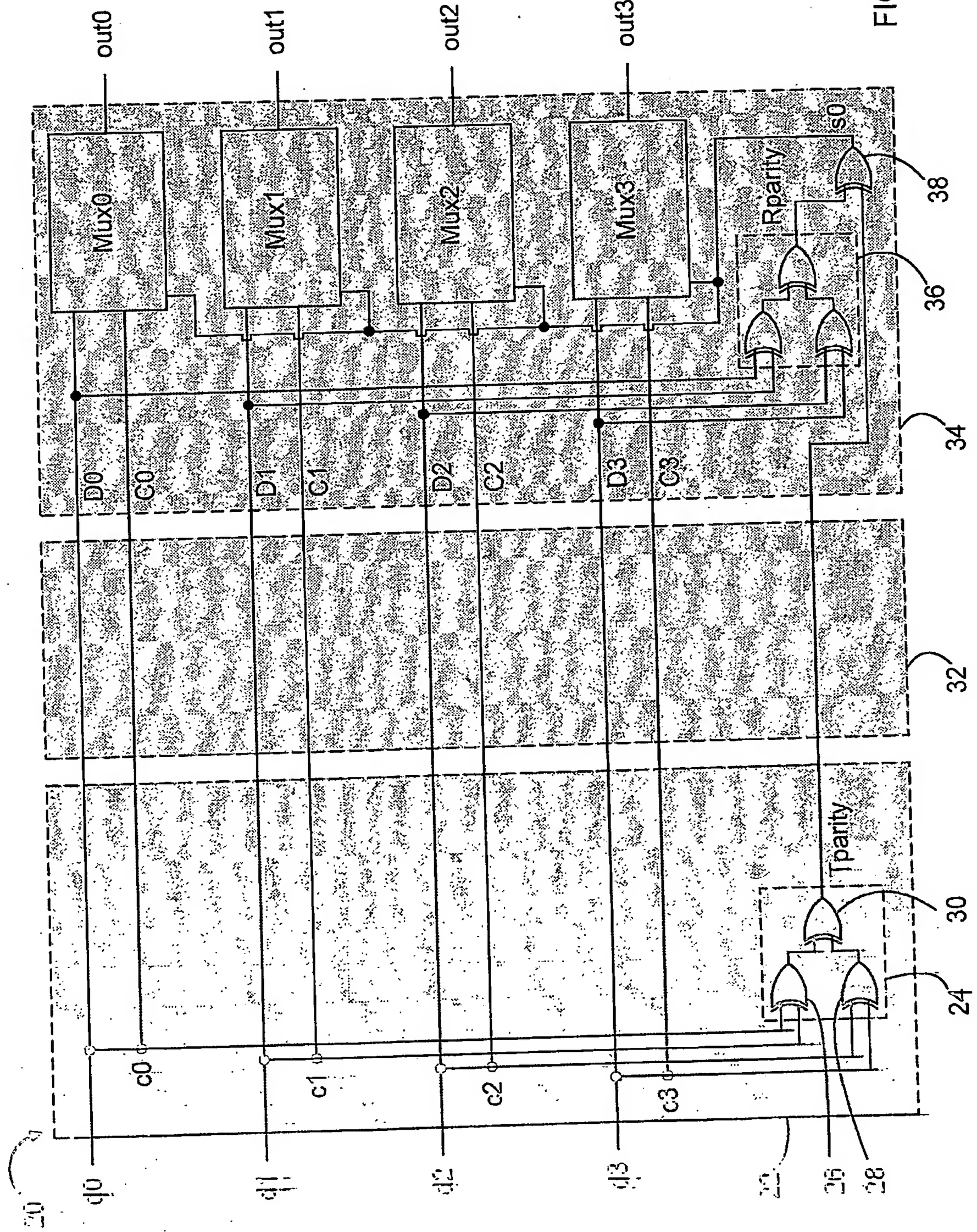
out0
out1
out2
out3
Mux0
Mux1
Mux2
Mux3
Rparity
s0
38
36
34
32
Tparity
30
24
D0
C0
D1
C1
D2
C2
D3
C3
c0
c1
c2
c3
d0
d1
d2
d3
20
26
28

FIGURE 2

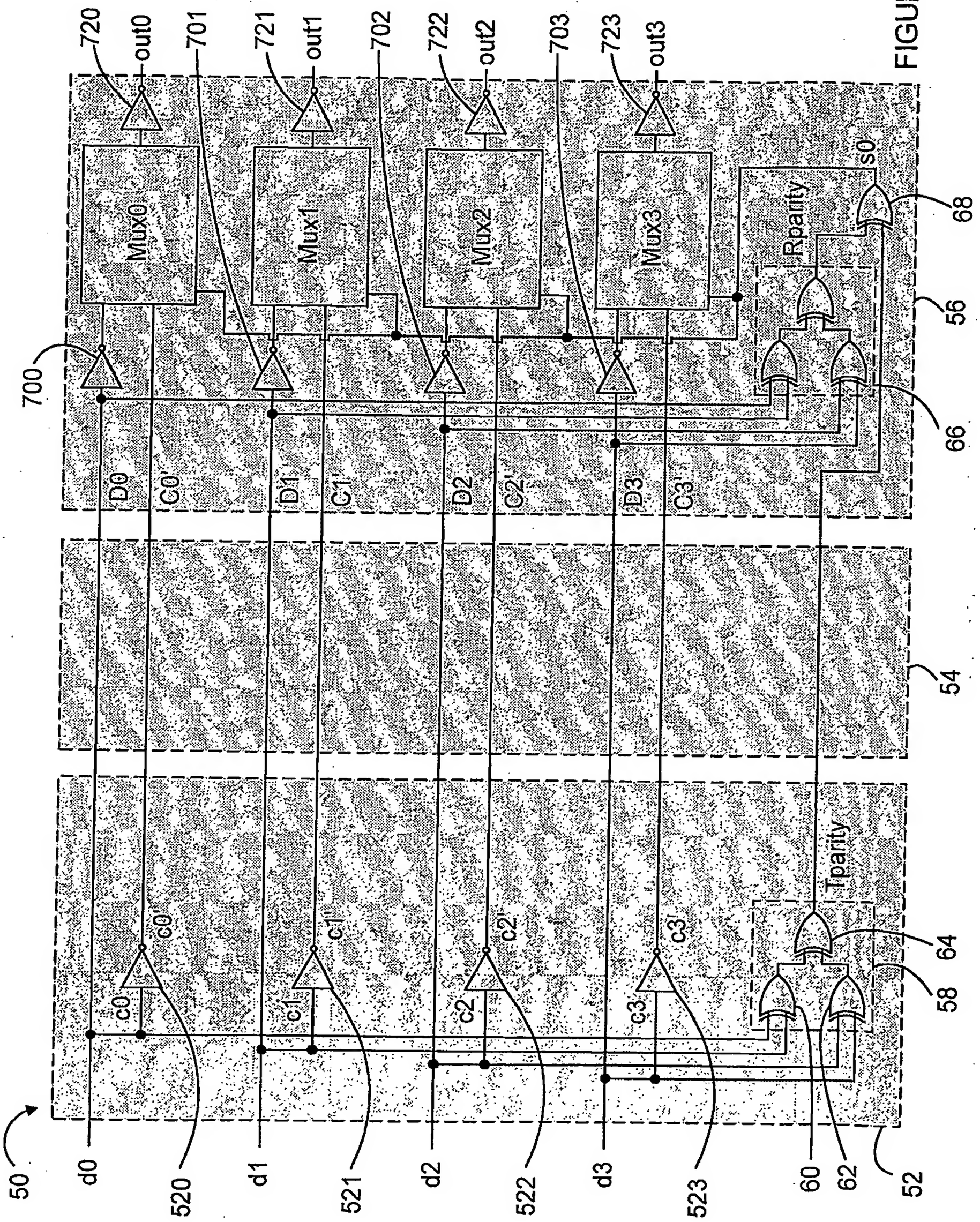
720
out0
701
721
out1
702
722
out2
703
723
out3
Mux0
Mux1
Mux2
Mux3
Rparity
S0
68
56
66
700
D0
C0'
D1
C1'
D2
C2'
D3
C3'
54
c0
c0'
c1
c1'
c2
c2'
c3
c3'
Tparity
64
58
62
60
52
50
d0
520
d1
521
d2
522
d3
523

FIGURE 3

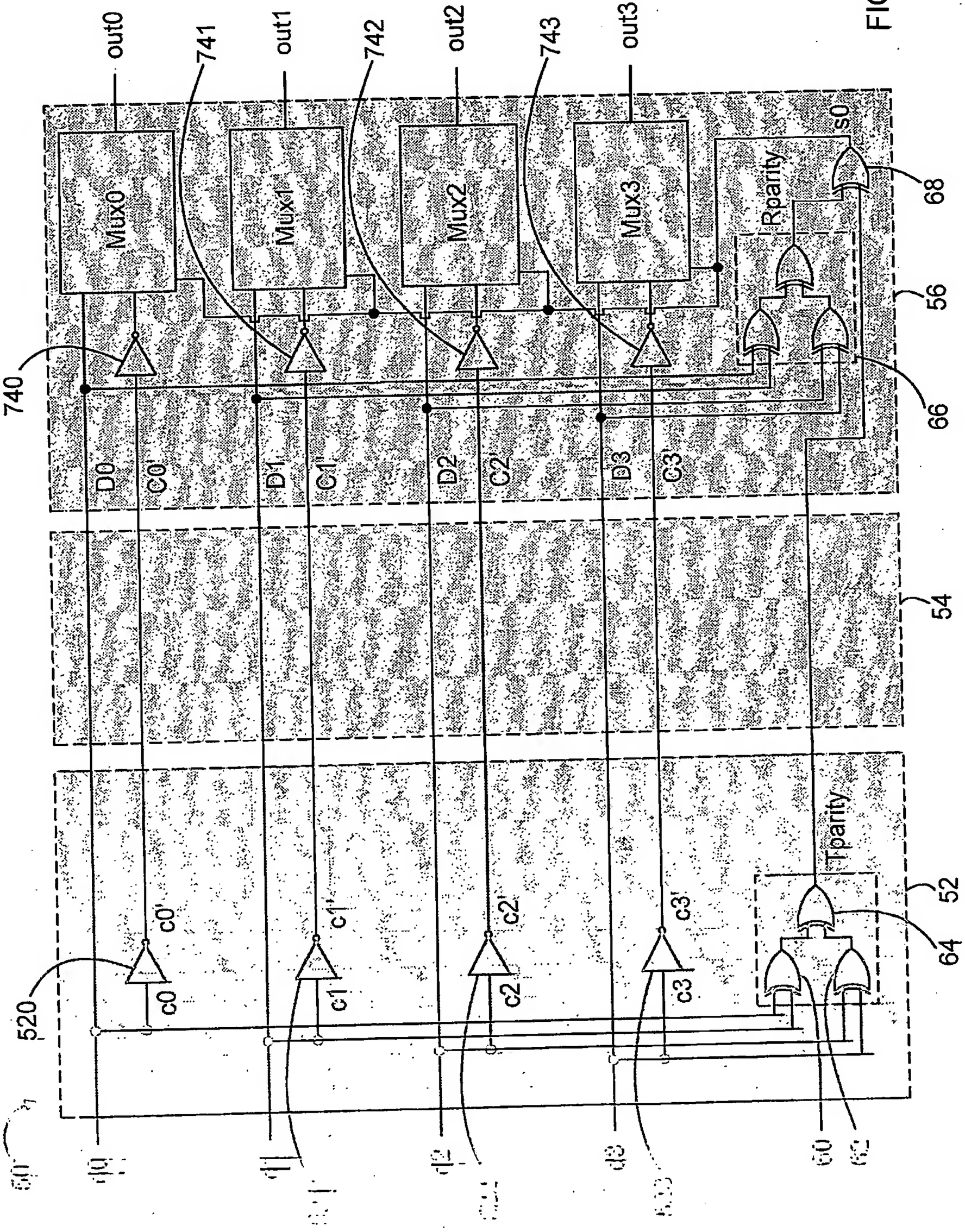
out0
741
out1
742
out2
743
out3
Mux0
Mux1
Mux2
Mux3
S0
Rparity
68
56
740
D0
C0'
D1
C1'
D2
C2'
D3
C3'
66
54
c0'
c1'
c2'
c3'
Tparity
52
64
520
c0
c1
c2
c3
60
62

FIGURE 4

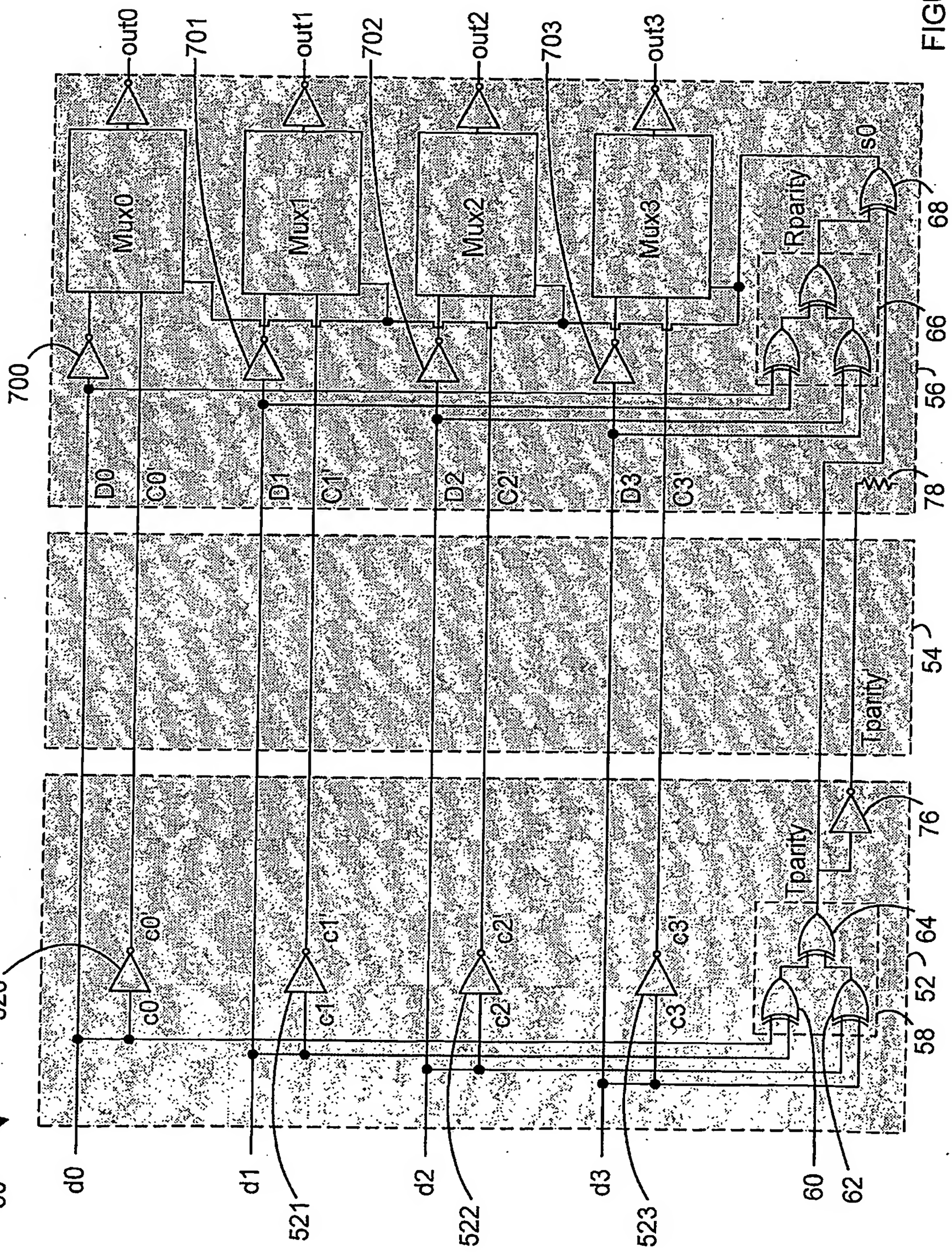
out0
701
out1
702
out2
703
out3
Mux0
Mux1
Mux2
Mux3
Rparity
s0'
68
700
D0
C0
D1
C1'
D2
C2'
D3
C3'
66
56
78
54
Tparity
76
64
52
58
520
c0'
c0
c1'
c1
c2'
c2
c3'
c3
521
522
523
d0
d1
d2
d3
50
60
62

FIGURE 5

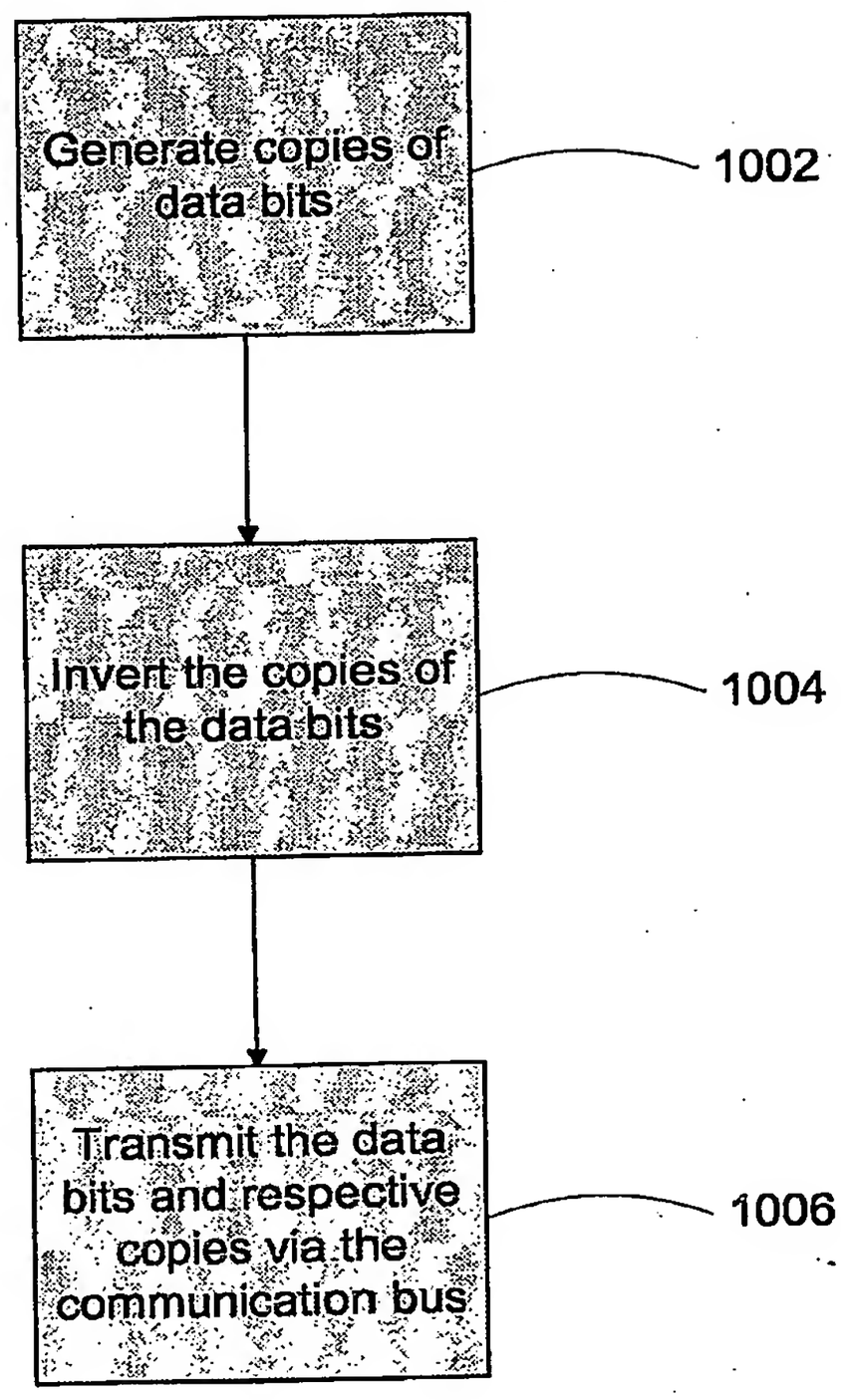
Generate copies of data bits
1002
Invert the copies of the data bits
1004
Transmit the data bits and respective copies via the communication bus
1006

FIGURE 6